QUESTION BANK

B.TECH (IV YEAR – I SEM) (2018-19)

Department of Electronics & Communication Engineering



MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956
(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)
Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

IV B.Tech I Semester Supplementary Examinations, February/March - 2018 VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70 Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B **** PART-A (22 Marks) When the channel is said to be pinched –off? [3] What are the different MOS layers? b) [4] Give the different scaling models and scaling factors? c) [3] State the disadvantages of dynamic CMOS logic? d) [4] What are the different levels of design abstraction at physical design? [4] e) What information from the targeted FPGA device is required in RTL f) synthesis? [4] PART-B (3x16 = 48 Marks)With neat sketches explain the CMOS n-well fabrication process indicating the 2. a) masks used. [8] b) What is threshold voltage of a MOS device and explain its significance. [8] 3. a) Discuss CMOS design style. Compare with nMOS design style? [8] Design a stick diagram for two input nMOS NAND and NOR gates? [8] Why scaling is required? Write the scaling factors for different types of device 4. a) parameters? [8] Discuss the limits due to sub threshold currents. [8] b) 5. a) Describe constructional features and performance characteristic of Pseudo-NMOS logic. [8] b) Explain two-phase clock generator using D flip-flops and draw the corresponding waveforms. [8] Write down the comparisons between Field Programmable Gate Array and Application Specific Integrated Circuit in detail. [8] Give the steps in ASIC design flow with flow diagram and briefly discuss about each step. [8] 7. a) Write down the step by step approach of FPGA design process on XILINX environment? [8] b) Design a queue and write the dataflow style VHDL program for the same. [8] **R13**

Code No: **RT41041**

Set No. 1

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours Max. Ma			
		Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****	
1.	a) b) c)	<u>PART–A</u> (22 Marks) Clearly explain about ION-IMPLANTATION step in IC fabrication. Why is VLSI design process presented in NMOS only? Justify with an example? Explain the formal estimation of CMOS Inverter delay.	[4] [4] [4]
	d) e) f)	Write a short note on clocked sequential circuits. Write a short note on clock mechanisms in VLSI design. List out the applications of FPGAs.	[3] [4] [3]
2.	a) b)	PART-B (3x16 = 48 Marks) Compare CMOS and Bipolar technologies. Explain the NMOS fabrication procedure.	[8]
3.	a) b)	Illustrate the lambda-based design rules with neat sketches. Design an area efficient layout diagram for the CMOS logic shown below $Y = \overline{(A+B+C)}$.	[8] [8]
4.	a) b)	What is meant by sheet resistance Rs? Explain the concept of Rs applied to MOS transistors. Calculate on resistance of an inverter from VDD to GND. If n- channel sheet resistance Rsn= $10^4\Omega$ per square and P-channel sheet resistance Rsp = 3.5×10^4	[8]
		Ω per square.(Zpu=4:4 and Zpd=2:2).	[8]
5.	a) b)	Give the subsystem design considerations of a four-bit adder. Explain step-by-step subsystem design approach. Consider an example.	[8]
6.	a) b)	Explain the terms (i) Static power dissipation (ii) Dynamic power dissipation. Discuss the VLSI design issues and design trends.	[8] [8]
7.	a) b)	Write about FPGA Programming Technologies in detail. Explain the step by step approach of FPGA design process on Xilinx environment.	[8] [8]

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

 Question paper consists of Part-A and Part-B	[4]			
Answer ALL sub questions from Part-A Answer any THREE questions from Part-B ****** ****** ****** ****** ******				
 a) Define threshold voltage of a MOS device and explain its significance. b) Discuss different forms of pull up, mentioning merits and demerits of each form: c) What is meant by standard unit of capacitance? Give some area capacitance calculations. d) Draw and explain fan-in and fan-out characteristics of different CMOS design Technologies. e) Give two reasons about the importance of package selection in VLSI design. f) Write a short notes on FPGA configuration and configuration modes. 2. a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating Saturation region. b) An nMOS transistor is operating in saturation region with the following parameters. VGS = 5V; Vtn = 1.2V; W/L = 110; μnCox = 110 μA/V². Fin Transconductance of the device. 				
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Transconductance of the device.				
3 a) Write a short note on "2um Double Metal Double Poly CMOS/RiCMOS rules	id [8]			
D. AL WITH A SHOULHOLD ON ZUIH DOUDIG WIGHAL DOUDIG LOLV CIVICAA/DICAVICA TUIGS	'. [8]			
Draw the circuit diagrams and the corresponding stick diagrams for nMOS and				
CMOS inverters.				
4. a) What are the alternate gate circuits are available? Explain any one of item wi	h			
suitable sketch.	[8]			
b) Implement the realization of gates using NMOS and PMOS.	50:			
	[8]			
5. a) Describe the nature of a parity generator and explain its structured designments	n [8]			
approach.b) Draw and give the design approach for a carry look ahead adder with it	ts			
structure.	[8]			
6. a) Write and explain about the sources of power dissipation in VLSI Design.	[8]			
b) Explain in detail about ASIC design flow with neat sketch.	[8]			
7. a) Draw and explain the routing architecture of field programmable gate arrays.b) Write about the shift register design and implementation onto FPGA.	[8]			

R13

Code No: **RT41041**

Set No. 3

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and **Instrumentation Engineering**)

Time: 3 hours Max. Marks: 70 Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B **** PART-A (22 Marks) 1. a) With neat sketch, explain drain characteristics of an n-channel enhancement MOSFET. [4] b) Compare and contrast the Lambda based and Micron based Rules for layout design. [4] Draw and explain the schematic of Pseudo-nMOS Inverter. [3] Explain the concept of driving large capacitive loads with, relevant examples. [4] List out the back-end steps in ASIC design flow. [3] Write about Programmable I/O blocks in FPGAs. [4] PART-B (3x16 = 48 Marks)With neat sketch explain BICMOS fabrication in an n-well process. 2. a) [8] Explain the term "aspects of MOSFET" in VLSI Design. b) [8] Tabulate the encoding scheme for a simple single metal CMOS/Bi-CMOS 3. a) process with respect to various MOS layers. [8] Draw the symbolic layout for the CMOS inverter and write the general CMOS logic gate layout guidelines. [8] Discuss the inverter delay and propagation delay. [8] 4. a) Write about the scaling limitations due to sub Supply voltages in MOSFETS. [8] Explain the architectural issues of subsystem design. [8] Explain the structural design approach with an example. b) [8] What is the need of testability? Explain design for testability. [8] 6. a) b) Explain about SoC design. [8] 7. a) Describe the shift register implementation using VHDL. [8] b) Explain about different programmable elements in FPGA architectures. [8]

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Code No: **RT41041**

Set No. 4

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 **VLSI DESIGN**

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

		Instrumentation Engineering)					
Ti	Time: 3 hours Max. Marks: 70						
		Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****					
		PART-A (22 Marks)					
1.	a)	Explain various regions of CMOS inverter transfer characteristics.	[3]				
	b)	Write a short note MOS layers and symbolic diagram translation to MASK form.	[4]				
	c)	Define and give the expressions for any four scaling factors of MOS device					
	ŕ	parameters.	[4]				
	d)	Write about general considerations in subsystem design processes.	[4]				
	e)	Write about technology options in VLSI design.	[3]				
	f)	Explain the need for FPGA and its applications.	[4]				
		$\underline{\mathbf{PART-B}}\ (3x16 = 48\ Marks)$					
2.	a)	Explain different forms of pull-ups used as load in CMOS enhancement.	[8]				
	b)	Determine pull-up to pull-down ratio of an NMOS inverter when driven through one or more pass transistors.	[8]				
3.	a)	Tabulate the encoding scheme for a simple single metal nMOS process with					
		respect to various MOS layers.	[8]				
	b)	What is stick diagram and explain about different symbols used for components					
		in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate.	[8]				
4.	a)	Describe three sources of wiring capacitances. Explain the effect of wiring					
		capacitance on the performance of a VLSI circuit.	[8]				
	b)	Write about the scaling limitations due to sub threshold currents in MOSFETS.	[8]				
5.		Realize the 2-i/p NAND gate using NMOS, PMOS and CMOS technologies.	[16]				
6.	a)	Discuss the design flow of system on chip design with neat sketch.	[8]				
	b)	Explain the steps of specification and logic design in ASIC design flow.	[8]				
7.	a)	Write the steps involved to prototype the HDL code onto FPGA device.	[10]				
	b)	List out the salient features of Xilinx 3000 CLB.	[6]				

IV B.Tech I Semester Supplementary Examinations, March - 2017 VLSI DESIGN

(Common to Electronics & Communication Engineering, and Electronics & Instumentation Engineering)

		instantentation Engineering)					
Time: 3 hours Max. Marks:							
	Question paper consists of Part-A and Part-B						
		Answer ALL sub questions from Part-A					
		Answer any THREE questions from Part-B					

		PART-A (22 Marks)					
1.	a)	Write down the equations for I_{ds} of an n-channel enhancement MOSFET					
1.	u)	operating in Non-saturated region and saturated region?	[4]				
	b)	Define stick diagram and layout diagram?	[4]				
	c)	Explain about the constraints in choice of layers.	[4]				
	ď)	Draw the basic structure of a dynamic CMOS gate?	[4]				
	e)	List out the back-end steps in ASIC design flow?	[3]				
	f)	List out the front-end steps in FPGA design flow?	[3]				
		$\underline{PART-B} (3x16 = 48 Marks)$					
2.	a)	Explain the nMOS enhancement mode fabrication process for different					
		conditions of V _{ds} ?	[8]				
	b)	Derive an equation for transconductance of an n-channel enhancement MOSFET					
		operating in active region.	[8]				
3.	۵)	Design a stick diagram and levent for two input CMOS NAND gate indicating					
Э.	a)	Design a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers.	[8]				
	b)	Explain 2µm Double Metal, Double Poly. CMOS / BiCMOS Rules.	[8]				
	U)	Explain 2µm Double Metal, Double Fory. CWO5 / BicWO5 Rules.	[O]				
4.	a)	What are the issues involved in driving large capacitor loads in VLSI circuit					
		regions? Explain.	[8]				
	b)	Calculate the gate capacitance value of 5mm technology minimum size transistor					
		with gate to channel value is $4 \times 10^{-4} \text{pF/mm}^2$.	[8]				
5.	a)	How switch logic can be implemented using Pass Transistors? Explain.	[8]				
	b)	Draw the transistor circuit diagram of shift register capable of holding and					
		shifting 4-bit word. Explain the circuit operation.	[8]				
6	۵)	What are EDC As? Explain the principle and apprecian	гот				
6.	a) b)	What are FPGAs? Explain the principle and operation.	[8]				
	U)	Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming.	[8]				
		purpose of 11 OA programming.	[0]				
7.	a)	Clearly explain each step of high level design flow of an ASIC.	[8]				
	,	Write a short note on mixed signal design?	[8]				

R13

Set No. 1

IV B.Tech I Semester Regular Examinations, November - 2016 VLSI DESIGN

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours Max. Marks: 70 Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B **** PART-A (22 Marks) 1. a) What are the steps involved in IC fabrication. [4] b) Draw the circuit diagram for CMOS two-input NAND gates. [4] c) Define Fan-in and Fan-out. [3] d) Write about pass transistor and pass transistor gates. [4] e) Write note on package solution. [4] f) What is the need of a FPGA? And write its applications. [3] $\underline{\mathbf{PART-B}} (3x16 = 48 Marks)$ 2. a) Explain about various IC technologies [8] b) Explain the term output conductance, using necessary equations. [8] 3. a) Design a stick diagram for NMOS EX-OR gate. [8] b) Draw the mask layout of 1-bit CMOS shift register cell. [8] 4. a) Define inverter delay? Explain. [8] b) Define scaling factor? Explain different types of device parameters. [8] 5. a) Explain the design of a 4-bit shifter. [8] b) Discuss the general arrangement of a 4-bit arithmetic process. [8] 6. a) Explain mixed signal design with neat sketch. [8] b) Discuss the clock mechanisms [8] 7. a) Explain the basic architecture of FPGA. [8] b) Explain the FPGA design process. [8]

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R13

Set No. 2

IV B.Tech I Semester Regular Examinations, November - 2016 VLSI DESIGN

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

22 Marks)

1.	a)	Explain the figure of merit of a MOS transistor.	[4]
	b)	What are scalable design rules and list its disadvantages.	[4]
	c)	What are the sources of wiring capacitances?	[3]
	d)	Explain charge storage.	[4]
	e)	What is testing? Explain.	[4]
	f)	Write the steps to design an FPGA.	[3]
		$\underline{\mathbf{PART-B}} \ (3x16 = 48 \ Marks)$	
2.	a)	Explain the MOS transistor operation with the help of neat sketches in the Enhancement mode.	[8]
	b)	Explain how the BiCMOS inverter performance can be improved.	[8]
3.	a)	What are the different types of design rules? Explain.	[8]
	b)	What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.	[8]
4.	a)	Explain briefly about sheet resistance?	[8]
	b)	Discuss the limits due to subthreshould current.	[8]
5.		Explain bus arbitration logic for n-line bus structured design approach.	[16]
6.	a)	Explain the single Stuck-at Fault model.	[8]
	b)	Discuss the ASIC design flow.	[8]
7.	a)	How to design FPGA-Based PCBs? Explain.	[8]
	b)	Write about FPGA families of different vendors.	[8]

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R13

Set No. 3

IV B.Tech I Semester Regular Examinations, November - 2016 VLSI DESIGN

(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

PART-A (22 Marks)

1.	a)	Draw the basic circuit of NMOS and CMOS inverter.	[4]
	b)	What are absolute design rules?	[4]
	c)	List out the limitations of scaling?	[3]
	d)	What is pre-charged bus concept?	[4]
	e)	Give the advantages and disadvantages of cell based design.	[4]
	f)	Write about configuration modes.	[3]
		$\underline{\mathbf{PART-B}} (3x16 = 48 Marks)$	
2.	a)	Derive the expression for the threshold voltage of MOSFET.	[8]
	b)	Explain the MOS transistor operation with the help of neat sketches in the Depletion mode.	[8]
3.		Draw the stick diagram and mask layout for CMOS two input NOR gate and stick diagram of two input NAND gates.	[16]
4.	a)	Discuss about nMOS transistor as a switch and pMOS transistor as a switch.	[8]
	b)	Define standard unit capacitance? Explain.	[8]
5.	a)	Explain two-phase clocking.	[8]
	b)	Discuss some system considerations.	[8]
6.	a)	Give the overflow of system on chip designs.	[8]
	b)	Explain the FPGA design flow.	[8]
7.		Explain stack implementation using VHDL.	[16]

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R13

Set No. 4

IV B.Tech I Semester Regular Examinations, November - 2016 **VLSI DESIGN**

(Common to Electronics & Communication Engineering and Electronics & **Instrumentation Engineering)**

Time: 3 hours Max. Marks: 70

> Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

> > ****

		<u>PART-A</u> (22 Marks)	
1.	a)	Compare CMOS with bipolar technologies.	[4]
	b)	Draw the circuit diagram for CMOS two-input NOR gates.	[4]
	c)	What are the advantages and disadvantages of dynamic logic?	[3]
	d)	Write about dynamic register element.	[4]
	e)	Write the steps to resolve the clock skew problem.	[4]
	f)	What parameters to be consider while identifying the FPGA?	[3]
		$\underline{PART-B} (3x16 = 48 Marks)$	
2.	a)	Explain different steps involved in the IC fabrication?	[8]
	b)	Draw the circuit for nMOS inverter and explain its operation and characteristics	[8]
3.	a)	Explain MOS layers with a neat sketch.	[8]
	b)	Explain 2µm CMOS design rule for wires?	[8]
4.	a)	What are the limits on logic levels and supply voltage due to noise in scaling?	[8]
	b)	Realize the NAND gate using nMOS technology.	[8]
5.	a)	Explain the structured design approach of parity generator.	[8]
	b)	Explain switch logic?	[8]
6.	a)	Discuss the design process for developing a chip.	[8]
	b)	Compare Full-Custom design with semi-custom design.	[8]
7.		Explain implementation of queue using VHDL.	[16]

1 of 1

MICROWAVE ENGINEERING MODEL QUESTION PAPERS

B.TECH (IV YEAR – I SEM) (2018-19)

Department of Electronics and Communication Engineering



MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956

(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)

Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

IV Year B. Tech ECE - I Sem

L T/P/D C 5 -/-/- 4

(R15A0421) MICROWAVE ENGINEERING

OBJECTIVES

- 1. To analyze micro-wave circuits incorporating hollow, dielectric and planar waveguides, transmission lines, filters and other passive components, active devices.
- 2. To Use S-parameter terminology to describe circuits.
- 3. To explain how microwave devices and circuits are characterized in terms of their "S" Parameters.
- 4. To give students an understanding of microwave transmission lines.
- 5. To Use microwave components such as isolators, Couplers, Circulators, Tees, Gyrators etc..
- 6. To give students an understanding of basic microwave devices (both amplifiers and oscillators).
- 7. To expose the students to the basic methods of microwave measurements.

UNIT I:

Waveguides & Resonators: Introduction, Microwave spectrum and bands, applications of Microwaves, Rectangular Waveguides-Solution of Wave Equation in Rectangular Coordinates, TE/TM mode analysis, Expressions for fields, Cutoff frequencies, filter characteristics, dominant and degenerate modes, sketches of TE and TM mode fields in the cross-section, Mode characteristics - Phase and Group velocities, wavelengths and impedance relations, Rectangular Waveguides – Power Transmission and Power Losses, Impossibility of TEM Modes ,Micro strip Lines-Introduction,Z0 Relations, losses, Q-factor, Cavity resonators-introduction, Rectangular and cylindrical cavities, dominant modes and resonant frequencies, Q-factor and coupling coefficients, Illustrative Problems.

UNIT II:

Waveguide Components-I: Scattering Matrix - Significance, Formulation and properties, Wave guide multiport junctions - E plane and H plane Tees, Magic Tee,2-hole Directional coupler, S Matrix calculations for E plane and H plane Tees, Magic Tee, Directional coupler, Coupling mechanisms - Probe, Loop, Aperture types, Wave guide discontinuities - Waveguide Windows, tuning screws and posts, Irises, Transitions, Twists, Bends, Corners and matched loads, Illustrative Problems.

Waveguide Components-II: Ferrites composition and characteristics, Faraday rotation, Ferrite components - Gyrator, Isolator, Circulator.

UNIT III:

Linear beam Tubes: Limitations and losses of conventional tubes at microwave frequencies, Classification of Microwave tubes, **O type tubes** - 2 cavity klystrons-structure, Reentrant cavities, velocity modulation process and Applegate diagram, bunching process and small signal theory Expressions for o/p power and efficiency, Reflex Klystrons-structure, Velocity Modulation, Applegate diagram, mathematical theory of bunching, power output, efficiency, oscillating modes and o/p characteristics, Effect of Repeller Voltage on Power o/p, Significance, types and characteristics of slow wave structures, structure of TWT and amplification process (qualitative treatment), Suppression of oscillations, Gain considerations.

UNIT IV:

Cross-field Tubes: Introduction, Cross field effects, Magnetrons-different types, cylindrical travelling

wave magnetron-Hull cutoff and Hartree conditions, modes of resonance and PI-mode operation, separation of PI-mode, O/P characteristics.

Microwave Semiconductor Devices: Introduction to Microwave semiconductor devices, classification, applications, Transfer Electronic Devices, Gunn diode - principles, RWH theory, Characteristics, Basic modes of operation - Gunn oscillation modes, LSA Mode, Introduction to Avalanche Transit time devices (brief treatment only), Illustrative Problems.

UNIT V:

Microwave Measurements: Description of Microwave Bench – Different Blocks and their Features, Precautions; Waveguide Attenuators – Resistive Card, Rotary Vane types; Waveguide Phase Shifters – Dielectric, Rotary Vane types. Microwave Power Measurement – Bolometer Method. Measurement of Attenuation, Frequency, VSWR, Cavity Q. Impedance Measurements.

TEXT BOOKS:

- 8. Microwave Devices and Circuits Samuel Y. Liao, PHI, 3rd Edition, 1994.
- 9. Microwave and Radar Engineering- M.Kulkarni, Umesh Publications, 1998.

REFERENCES:

- 1. Foundations for Microwave Engineering R.E. Collin, IEEE Press, John Wiley, 2nd Edition, 2002.
- 2.Microwave Circuits and Passive Devices M.L. Sisodia and G.S.Raghuvanshi, Wiley Eastern Ltd., New Age International Publishers Ltd., 1995.
- 3. Microwave Engineering Passive Circuits Peter A. Rizzi, PHI, 1999.
- 4. Electronic and Radio Engineering F.E. Terman, McGraw-Hill, 4th ed., 1955.
- 5.Elements of Microwave Engineering R. Chatterjee, Affiliated East-West Press Pvt. Ltd., New Delhi,1988.

OUTCOMES

- 1. Understand the significance of microwaves and microwave transmission lines
- 2. Analyze the characteristics of microwave tubes and compare them
- 3. Be able to list and explain the various microwave solid state devices
- 4. Can set up a microwave bench for measuring microwave parameters

MODEL PAPER –I

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations

MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75marks

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE

Questions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART A (25

Marks)

1.

a) Name different electromagnetic frequency spectrum region and microwave band designations for CCIR/IEEE/US military bands.

[2M]

b) List out the advantages of micro-strip line over rectangular wave guide.

[3M]

c) What are ferrites and give their properties?

[2M]

d) Explain about Tuning ports.

[3M]

e) State the limitations of conventional tubes at microwave frequencies.

[2M]

f) Differentiate between klystrons and TWT.

[3M]

g) What is the difference between travelling wave tube and magnetron?

[2M]

h) Discuss various operating mode of Gunn diodes.

[3M]

i) Write short notes on "Properties of S - matrix".

[2M]

i) Under what conditions double minimum method of VSWR is preferred?

[3M]

Part B 50 Marks

2. What are the advantages and applications of microwave frequencies? Discuss in detail.

- 3. Prove that a cavity resonator is nothing but an LC circuit.
- 4. What is Faraday rotation? Explain the working of a ferrite circulator with neat sketches. How can it be used

as an isolator?

(OR)

- 5. Show the attenuation produced by rotary vane attenuator is given by $40 \log (\sin \theta)$.
- 6. Draw the equivalent circuit of reflex klystron & explain about the electronic admittance of it and calculate

the efficiency.

(OR)

- 7. Derive the expression for power gain in dB for TWT.
- 8. Explain how magnetron allows electron bunching to take place and prevents favored electrons from slipping

away from their relative position.

(OR)

- 9. What is a TRAPATT diode? How is it better than IMPATT diode?
- 10. Derive the S-matrix of a directional coupler in standard form.

(OR

11. Explain the Attenuation measurement techniques.

MODEL PAPER –II

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75marks

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART A (25

Marks)

1.

a) Determine the cut – off frequency of the dominant mode for an air filled rectangular WG when a/b = 2 with a = 4cm.

[2M]

b) Define the quality factor of a resonator.

[3M]

c) Calculate the attenuation of a rotary Vane attenuator if the angle of rotation is 34 degrees.

[2M]

d) Explain about bends, corners.

[3M]

e) Define velocity modulation.

[2M]

f) What are the characteristics of TWT?

[3M]

- g) What is strapping in magnetron? How is the same effect obtained without strapping? [2M]
- h) Write short notes on "LSA mode in GUNN diode".

[3M]

i) What is scattering matrix? Explain the significance of S - matrix.

[2M]

j) Explain in brief about errors in microwave power measurement?

[3M]

Part B 50

Marks

2. What is a Microwave spectrum bands? Explain briefly the Applications of Microwave waves at various frequency bands.

- 3. Derive the Characteristic impedance of a micro strip lines.
- 4. Write short notes on the following.
 - (a) Directional couples.

- (b) Waveguide windows.
- (c) Flap attenuator.

- 5.a) Write short notes on "Cavity resonators"
- b) Distinguish between TEM, TE and TM modes of the propagation in rectangular waveguides.
- 6. Show that input admittance of triode circuit is given by $\omega^2 L_K C_{gk} g_m + j\omega C_{gk}$ considering the inter electrode capacitances, lead inductance.

(OR)

- 7. a) What is a slow wave structure? Explain and differentiate between different structures.
 - b) Explain the working principle of TWT amplifier.
- 8. a) Draw the characteristics of TRAPATT diode and explain their shape.
- b) Explain different types of modes for uniformly doped bulk diodes with low resistance contacts.

(OR)

- 9. Derive the Hull cutoff Voltage for a magnetron.
- 10. a) What are the precautions to be taken while setting up microwave bench for measurement of various parameters?
 - b) How do you measure microwave power using a Bolometer.

- 11. Write short notes on
 - (a) Properties of S matrix.
 - (b) Gyrator and its applications.

MODEL PAPER -III

MALLA REDDY COLLEGE OF ENGINEERING AND **TECHNOLOGY**

IV B.Tech I Semester Examinations MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75marks

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Ouestions.

Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART A (25)

Marks)

1. a) What is meant by the dominant mode of a waveguide? What is the dominant mode in rectangular wave guide?

[2M]

b) List few applications of a cavity resonator.

c) Explain About Isolator.

d) Differences between Transmission lines and micro strip lines.

e) Distinguish between O – type tubes and M – type tubes.

f) How are oscillations avoided in travelling wave tube?

g) Explain the terms of frequency pulling and frequency pushing with reference to a magnetron.

[2M]

h) Compare IMPATT and TRAPATT diodes.

i) Differentiate between transferred electron devices and transistors.

j) State the various methods for measuring attenuation?

[3M]

PART B **(50**

Marks)

2. Derive the expressions for cut off frequency, phase constant, group velocity, phase velocity and wave impedance in rectangular waveguide, for TE modes.

(OR)

- 3. Explain the losses in Micro strip lines.
- 4. (a) Write short notes on "Cavity resonators".
 - (b) Distinguish between TEM, TE and TM modes of the propagation in rectangular wave guides.

- 5. Explain the construction, operation and applications of the following microwave components.
 - (a) Circulator
 - (b) Gyrator.
- 6. Describe the mechanism of velocity modulation in a two cavity Klystron and hence obtain an expression for the bunched beam current?

- 7. What is need of Helix in TWT? Describe the Amplification process for TWT.
- 8. Write short notes on "Magnetron Oscillator", and its applications.

OR)

- 9 a) Write short notes on "LSA mode in GUNN diode".b)How is it possible to exhibit negative resistance characteristics in an IMPATT diode?
- 10. What is magic Tee? Describe the properties of magic Tee, giving its S-Matrix.

- 11.a) Explain VSWR measurement in detail.
 - b) Calculate VSWR of a rectangular guide of 2.3cmx1.0cm operating at 8GHz. The distance between twice minimum power points is 0.09cm.

MODEL PAPER -IV

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75marks

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Ouestions.

Choosing ONE Question from each SECTION and each Question carries 10 marks.

Part A (25

Marks)

1)

(a) Determine the group velocity and phase velocity for a dominant mode propagating through a waveguide of breadth 10cms at frequency 2.5GHz.

[2M]

(b) How are waveguides different from normal two wire transmission lines? Discuss the similarities and dissimilarities.

[3M]

(c) Explain About Gyrator.

[2M]

(d) Derive the Quality factor of a cavity resonator.

[3M]

(e) What are the Types of slow wave structures?

[2M]

(f) What is a Magic Tee? Why it is called as Magic Tee?

[3M]

(g) Explain resonant modes in magnetron.

[2M]

(h) Draw the graph between negative resistances versus transit angle and explain its Shape.
[3M]

(i) Explain the principle of E Plane.

[2M]

(j) Define Voltage standing wave ratio and Reflection coefficient.

[3M]

Part B (50

Marks)

2) Derive the wave equations for TM mode in Rectangular Wave guide.

(OR)

3) Explain about dominant and degenerate modes. Draw the sketches of TE and TM mode analysis.

- 4) a) An X band waveguide filled with a dielectric is operating at 9GHz. Calculate the phase and group velocities in the wave-guide. Take \mathcal{E}_r as 2.25 for the dielectric.
 - b) What are cavity resonators? What are their most desirable properties?

- 5) What is the need for phase shifters at microwave frequencies? Explain the concept of realizing phase shifting through Dielectric Materials.
- 6) Define and explain the significance of the following terms as applicable to a directional coupler.
 - i. Coupling
 - ii. Directivity
 - iii. Insertion loss

(OR)

- a) With the aid of neat sketches, describe the construction and operation of TWT.b) Starting with the assumption that there are three forward traveling waves in TWT, derive an expression for power gain of the tube.
- 8) a) How does the reflex Klystron work? Discuss its operating characteristics and applications?
 - b) Distinguish between velocity modulation and current modulation. Derive an expression for minimum distance at which maximum bunching occur in Klystron amplifier.

(OR)

- 9) a) With neat schematics, describe the 2-valley model theory, and its applicability For n-type GaAs, specifying the parameter values involved.
 - b) Compare the merits and demerits of TEDs and Avalanche Transit Time Devices.
- 10) a) List out the microwave applications of TWTs, bringing out their merits and demerits.
 - b) Describe the need and process of Strapping of Magnetrons, distinguishing between single and double ring straps. Sketch the variation of operating wavelength with mode number, in such cases.

(OR)

11) What are scattering parameters? Derive the formation of scattering matrix and explain the properties.

MODEL PAPER -V

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75marks

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE

Questions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART A (25

Marks)

1a)Compare the differences between Waveguide and Co-axial cable.

[2M]

b)What are the coupling coefficients of cavity resonator

[3M]

c)Explain about circulator.

[2M]

d)Define the following in directional couplers:

[3M]

i.Coupling factor ii.Directivity iii.Isolation

e)What are the performance characteristics of a klystron amplifier?

[2M]

f)What is the difference between travelling wave tube and magnetron?

[3M]

g)What are the types of M-type tubes?

[2M]

h)Compare IMPATT and TRAPATT diodes.

[3M]

i)Explain the principle of H Plane.

[2M]

j)Draw the microwave setup using slotted line to measure VSWR.

[3M]

Part B (50 Marks)

2. Show that the TEM, TM₀₁&TM₁₀ modes does not exist in a rectangular waveguide.

(OR)

- 3. a) What are Power Transmission and Power losses in Rectangular wave guide.
 - b) Derive the Quality Factor of a rectangular cavity resonator.
- 4. a) Explain the concept and merits of a micro strip line transmission.
 - b) Discuss the properties of micro strip lines.

- 5. a) Describe the working of a Rotary Vane Attenuator, with neat schematic.
 - b) Write short notes on:

i. Tuning Screws

ii.Tuning Posts

iii.Bends

iv.Phase Shifters

- v.Terminations
- 6. a) What is transit time effect? What is the importance of this transit time in microwave tubes? Can we use vacuum tubes at microwave frequencies?
 - b) A reflex Klystron uses an accelerating voltage of 300V and operates at a frequency of
 - 2GHz. Power output maxima are found to occur at reflector voltages of -8 Volts,-

Volts and 360 volts. Identify the transit times of the observed modes?

(OR)

7. a) An O type TWT operates at 2GHz. The slow wave structure has a pitch angle of 4.4°

and attenuation constant of 2 Np/m. Determine the propagation constant of the traveling

wave in the tube.

- b) Write short notes on "Helix traveling wave tube".
- 8. a) A magnetron is operating in the Pi mode and has the following specifications, N=10,

f=3MHz, a=0.4cm, b=0.9cm, l=2.5cm, $V_0=18KV$, B=0.2 wb/m². Determine

- i. The angular velocity of the electron.
- ii. The radius at which radial forces due to electric and magnetic fields are equal and opposite.
- (b) What are Hartree harmonics? Explain in detail.

(OR)

9. a) Explain the GUNN effect in semiconductor devices. Discuss how it leads to negative

resistance and hence oscillations at Microwave frequency.

- b) Write short notes on "IMPATT diode".
- 10. a) Explain the principle of working a H-Plane Tee Junction with neat schematics.
 - b) Explain how a Magic Tee can be used as an Isolator.

- 11. a) Describe the procedure for measurement of Q of a cavity.
 - b) Draw a setup for measurement of power in laboratory and explain the function of each block and procedure of measurement.

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3	B. Tecli	IV.Year I Semester CELLULAR ÄN	Examinations,	November/Dece MUNICATION	imber - 2016 S	13	MB
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	f)What is the g):What is me h) Write short	ant by foliage? Defin minimum separation ant by frequency ma notes on sectorization	n required between magement in the contract of	i M	nas? Explain :	briefly.[3] :::[2] [3]	M3
		ant by hand-off and concept of delaying				[2] [3]	×
	Н З	Na N	PART-B	3 N:		. : ···:: (50·Marks)	M3
	What are the any two.	ne various technique		the capacity of a	cellular syste	em? Explain [10]	
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		t notes on: i) space					
3	b)Discuss ho	w antenna height eft	ects the coverage	and interference	e of cellular	system [5+5]	
	6.a) Discuss the	e merits of point to pe effect of propagation		als over water.		[5+5]	
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3	7.a) : :::Explain b) : ····Explain	umbjella antenr in detail about l	na patteriis in det	OR ail. · ppagation:	NS		MS
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		re the various hat hort notes on: i)			ain any two in br	ief. [5+5]	
3	1 La)How consider	an handoff be in ering signal at tw	nitiated at the boo	OR	cells, based upor	threshold point	MS
	b) What i rate?	s meant by a dr	opped call? Wh	at are the factor	s that influence	the dropped call [5+5]	
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MODEL PAPER –I

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations

CELLULAR AND MOBILE COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

	PART-A	25 Marks
1) a)	Mention the elements of basic cellular systems.	[2M]
b)	What is interference and co-channel interference?	[3M]
c)	Comment on the lowering antenna height method in a valley.	[2M]
d)	What is channel combiner?	[3M]
e)	What are the three main types of point-to-point model?	[2M]
f)	Define space diversity technique.	[3M]
g)	What is meant by frequency management?	[2M]
h)	Define paging channel.	[3M]
i)	Draw a simple two-level handoff scheme diagram.	[2M]
j)	Define dropped call.	[3M]
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PART-B 50 Marks

- 2) a) What are the limitations of conventional mobile telephone system? Describe the various Generations of wireless mobile communication?
 - b) What are the Main advantages and disadvantages of various cellular structures?

(OR)

- 3) a) What is the need of Frequency reuse? Prove that for a hexagonal geometry the cochannel reuse ration is (3N) $^{1/2}$ where N= i^2+ij+j^2 .
 - b) Determine the number of cells in cluster for the following values of the shift Parameters I and j in a regular hexagon geometry pattern:
 - (i) i=2 and j=4
- (ii) i=3 and j=3
- 4) a) What are the different interferences in cellular systems? Explain each with diagrams
 - b) Explain how a diversity receiver reduces the interference.

- 5) Discuss in detail
 - a) The propagation in near distance
 - b) Long distance propagation

- 6) a) Explain the effects of human made structures for mobile propagation in open area.
 - b) What is mean by foliage? Explain Foliage loss.

- 7) a) Explain the sum-and-difference patterns and their synthesis in detail.
 - b) Explain the design aspects and merits of an omni-directional antenna in cell site.
- 8) Describe the concept of frequency management concern to numbering the channels and Grouping into the subset

(OR)

- 9) Explain the channel assignment to the cell sites based on the adjacent channels.
- 10) a) What are the various methods of delaying handoff? Explain briefly.
 - b) What is meant by dropped call? Explain the factors that influenced dropped call rate.

(OR)

11) What are the various handoff strategies based on algorithms of handoff? Explain in detail.

MODEL PAPER-II

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations

CELLULAR AND MOBILE COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

	PART-A	25 Marks
1)		
a)	How voice quality can be tested.	[2M]
b)	What are advantages of frequency reuse?	[3M]
c)	Define co-channel interference.	[2M]
d)	What is known as near end-far-end interference?	[3M]
e)	Write a short note on signal reflections in a flat terrain.	[2M]
f)	Write short note on umbrella antenna pattern.	[3M]
g)	Define voice channel and SAT?	[2M]
h)	What is meant by fixed channel assignment?	[3M]
i)	What are the types of handoff?	[2M]
j)	Write short note on inter system handoff.	[3M]

PART-B 50 Marks

2) a) Describe the principle of Operation of cellular mobile system and explain the cellular Concept with neat diagram.

(OR)

- 3) a) What are the various components in a cellular system? Explain.
 - b) List the various techniques used to expand the capacity of a cellular system
- 4) a) How the interference is different from noise in cellular system? explain
 - b) What are the different types of interference for a cellular system in detail?

(OR)

- 5) a) Explain the types of non-co-channel interferences in cellular system.
 - b) Distinguish Co-channel interference and Non Co-channel interference.
- 6) a) Describe the form of a point to point model and explain its types.
 - b) Explain the mobile signal propagation over water and flat area

(OR)

7) a) What is known as directional antennas? Explain directional antennas for interference in detail.

- b) Explain space diversity antennas in detail.
- 8) What is the important concerning of frequency management chart? Give the structure of the channels in 800 MHz system with frequency ranges?

- 9) Explain clearly different channel assignments and its importance in mobile communications or in brief frequency management in mobile communications?
- 10) a) What is meant by handoff? describe the classification of handoff process?
 - b) What is meant by handoff initiation? Explain different methods of Handoff initiation with suitable diagrams.

- 11) a) Explain about the handoff and power control?
 - b) Explain about inter MSC Handoff?

MODEL PAPER -III

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations

CELLULAR AND MOBILE COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

	PART-A	25 Marks
1)		
a)	What is known as circuit merit?	[2M]
b)	Define cell splitting.	[3M]
c)	What are the types of diversity?	[2M]
d)	What is frequency-agile combiner?	[3M]
e)	Write the equation of effective antenna height gain.	[2M]
f)	What is known as abnormal antenna configuration?	[3M]
g)	Write short note on set-up channels.	[2M]
h)	Differentiate channel sharing and borrowing.	[3M]
i)	Define soft handoff.	[2M]
j)	What is a MAHO?	[3M]

PART-B 50 Marks

- 2) a) Briefly describe the concept of mobile radio environment.
 - b) What are the advantages of digital cellular system over analog cellular system?

(OR)

- 3) a) Derive the desired C/I for a Normal case in an Omni directional antenna system
 - b) Explain about mobile fading characteristics.
- 4) a) What are the different types of Non co-channel interference in a cellular system? Explain
 - b) Explain the effects of antenna design Parameters for the interference in a cellular system

(OR)

- 5) a) Explain the co-channel interference reduction factor and derive the general formula for C/I.
 - b) What are the various techniques to measure CCI? Explain in detail
- 6) a) Explain the mobile radio propagation over water and flat open area and write the general expression.
 - b) Describe the effect of antenna height in near and long distance mobile propagation.

- 7) Explain
 - a) Umbrella pattern antenna.
 - b) Space diversity antennas.
- 8) Describe the grouping of the voice, set-up and paging channels.

- 9) Explain in detail the fixed channel and non fixed channel assignment?
- 10) a) Explain different handoff strategies and its importance in different situations.
 - b) How to improve call drop rate.

- 11) Write a short notes on
 - a) Forced Handoff
 - b) Inter System Handoff

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MODEL PAPER –IV

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations

CELLULAR AND MOBILE COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Ouestions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

	PART-A	25 Marks
1)		
a)	Define fading effect.	[2M]
b)	What is meant by first-tier of interference?	[3M]
c)	If co-channel interference reduction factor q is 6 what will be the cluster site?	[2M]
d)	What is cross talk?	[3M]
e)	Draw the diagram of human made structures to find propagation path loss curve.	[2M]
f)	What is meant by difference pattern?	[3M]
g)	What is known as FOCC?	[2M]
h)	Define sectorization.	[3M]
i)	Comment on two-hand off level algorithm.	[2M]
j)	What is known as delaying handoff?	[3M]
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PART-B 50 Marks

- 2) a) What is the uniqueness of mobile radio environment? Explain.
 - b) Explain the significance of fading of fading in mobile environment.

(OR)

- 3) a) Explain Cell splitting and Concept of frequency channels
 - b) Explain co-channel interference with first tier and second tier example
- 4) a) Derive the expression for carrier to interference Ratio in a cellular system for a normal case and worst case scenario with an Omni directional antenna.
 - b) Determine the minimum cluster size for a cellular system designed with an acceptable value of C/I=18dB. Assume the path Loss exponent as 4 and co channel interference at the mobile unit from 6 equidistant cells in the first tier.

- 5) a) Explain the causes for near to far end interference.
 - b) Mention different systems to reduce the interference.
- 6) a) Explain the effect of antenna pattern on the interference at the base station and mobile unit .

b) Explain in detail about near and long distance mobile propagation

(OR)

- 7) a)Describe the various steps involved in finding antenna height gain in mobile environment b) Explain umbrella pattern antenna and Omni-directional antennas in detail.
- 8) Write short notes on
 - a) channel sharing and barrowing
 - b) Fixed channel assignment

(OR)

- 9) What type of messages is received to the setup channels when mobile unit monitors strongest signal strength?
- 10) a) Write notes on power difference handoffs
 - b) Explain a two level handoff scheme with suitable example

(OR)

11) a) What is meant by call drop? Explain and suggest methods to reduce call drop rate. b) Write short notes on different types of hand off mechanisms.

MODEL PAPER-V

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

IV B.Tech I Semester Examinations

CELLULAR AND MOBILE COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions,

Choosing ONE Question from each SECTION and each Question carries 10 marks.

	PART-A	25 Marks
1)		
a)	Give two advantages of cellular mobile systems over telephone systems.	[2M]
b)	Define micro cells.	[3M]
c)	If co-channel interference reduction factor q is 5.2 and the cluster size is q what will be	
	the carrier to interference ratio.	[2M]
d)	What are the methods to reduce adjacent channel interferences?	[3M]
e)	Draw the simple model for propagation over water.	[2M]
f)	Write short note on high-gain broadband umbrella pattern antenna.	[3M]
g)	Write short note on non-fixed channel assignment.	[2M]
h)	What is known as access channels?	[3M]
i)	What is known as dropped call rate?	[2M]
j)	Write short note on initiation of handoff.	[3M]
	DADT D	50 Marilia

PART-B 50 Marks

- 2) a) What is the uniqueness of mobile radio environment? Explain.
 - b) Explain the call initialization, call progress and call termination process.

(OR)

- 3) a) Explain the normal case of carrier to interference ratio with Omni-directional antenna. b) What is cell-splitting? Explain its types in detail
- 4) a) discuss in details the various techniques to measure co channel interference, prove that the real time co channel interference measurement is difficult to achieve

- 5) a) Explain non-co-channel interference effects on coverage and interferences.
 - b) Explain the effects of coverage and interference by power decrease and decrease antenna height.
- 6) a) What are the different propagation models available for mobile communication, Explain?
 - b) Explain the phase difference between direct and reflected paths in detail.

- 7) Explain about minimum separation of cell-site receiving antennas
- 8) Elaborate dynamic channel assignment and compare its advantages and disadvantages with the fixed channel assignment

(OR)

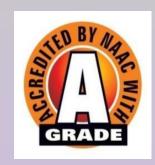
- 9) What is known as dynamic channel assignment average blocking and handoff blocking? Explain.
- 10) a) Explain MAHO and soft handoff techniques.
 - b) Explain "Dropped call rate" in detail.

- 11) Write a short note on
 - a) Delayed handoff
 - b) Inter systems Handoff
 - c) Power difference Handoff

MALLAREDDY COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)







QUESTION BANK

(COMPUTER NETWORKS)

By

Dr. C. Ravi Shankar Reddy

Dr. R. Murageshan

Miss. G. Anusha

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY IV Year B.Tech. ECE-I Sem L T/P/DC

4 1/-/-3

(R15A0514) COMPUTER NETWORKS

OBJECTIVES:

The students will be able to:

- 1. Build an understanding of the fundamental concepts of computer networking.
- 2. Familiarize the student with the basic taxonomy and terminology of the computer networking area.
- 3. Introduce the student to advanced networking concepts, preparing the student for entry Advanced Courses in computer networking.
- 4. Allow the student to gain expertise in some specific areas of networking such as the design and Maintenance of individual networks.

UNIT I:

Introduction: Introduction to networks, Internet, Protocols and Standards, The OSI model, Layers in OSI Model, TCP/IP Suite, Addressing.

Physical Layer: Physical Layer Introduction, Transmission media.

UNIT II:

Data link layer: Introduction, Cyclic codes, checksum, Framing, Flow and error control, HDLC, Point to point protocols

Media Access Sub Layer: Random Access, Controlled access, channelization

UNIT III:

Ethernet, Fast Ethernet, Giga bit Ethernet, wireless LANS, Connecting lans, Backbone networks, Virtual lans, Wireless wans

UNIT IV:

Network Layer: Logical addressing, internetworking, tunneling, address mapping, ICMP, IGMP, Forwarding, Unicast routing protocols, multicast routing protocols

UNIT V:

Transport Layer: Process to process delivery, TCP and UDP protocols, SCTP ,Data traffic , congestion, Congestion Control, QoS, integrated services, Differentiated services, QoS in Switched networks.

Application Layer: Domain name space, DNS in internet , Electronic Mail, FTP, WWW, HTTP, SNMP

TEXT BOOKS:

- 1. Data Communications and Networking- Behrouz A Forouzan Fourth Edition TMH, 2006.
- 2. Computer Networks- Andrew S Tanenbaum, 4th Edition, Pearson Education

REFERENCE BOOKS:

- 1. An Engineering approach to computer Networks- S.Keshav, 2nd Edition, Pearson Education
- 2. Computer and communication Networks- Nader F Mir, Pearson Education
- 3. Data and Computer Communications, G.S.Hura and M. Singhal, CRC Press, Taylor and Francis Group.
- 4. Data Communications and Computer Networks, P.C. Gupta, PHI
- 5. Computer Networking : A top-down Approach Featuring the Internet, James F.Kurose, K.W.Rose, 3rd Edition, Pearson Education

OUTCOMES:

- 1. Have a good understanding of the OSI Reference Model and in particular have a good knowledge of Layers 1-3.
- 2. Analyze the requirements for a given organizational structure and select the most appropriate networking architecture and technologies
- 3. Specify and identify deficiencies in existing protocols, and then go onto formulate new and better protocols
- 4. Have an understanding of the issues surrounding Mobile and Wireless Networks.
- 5. Have a working knowledge of datagram and internet socket programming

MODEL PAPERS

Time: 3hours

MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY (Autonomous Institution – UGC, Govt. of India)

B. Tech IV Year I Semester Examinations Computer Networks

(Electronics Communication and Engineering)

Max Marks: 70

Note: This question paper contains **two questions from each of** five Units. Answer **any one full** question from each unit. Each question carries 14 marks and may have a, b, c as sub questions.

1.	Explain ISO OSI Reference model with neat sketch. (OR)	(14M)
2.	Explain different kinds of Transmission Media.	(14M)
3.	Explain CSMA and CSMA/CD in detail. (OR)	(14M)
4.	a) What do you mean by bit stuffing and why it is employed.b) Explain error detection using Checksum.	(7M) (7M)
5.	a) Compare and contrast TDM, STDM and FDM.b) What are the common Fast Ethernet implementations? Give the purpose of NIC (OR)	(14M) (7M)
6.	a) Explain indetail about different Bluetooth layers.b) wWhat are the advantages of dividing an Ethernet LAN with a bridge? Give the relation between a switch and a bridge	(7M) aship (7M)
7.	a) With the aid of necessary explain in detail about significance of tunneling.b) Explain DHCP.(OR)	(7M) (7M)
8.	a) Write short notes on Link state routing.b) Explain the process of physical address to logical address mapping using Boot Strap Protocol.	(7M) (7M)
9.	a) Explain UDP header format.b) Write short notes on congestion control.(OR)	(7M) (7M)
10.	Explain the following a) FTP b) DNS	(7M) (7M)

Code No: R15A0514

MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY (Autonomous Institution – UGC, Govt. of India)

B. Tech IV Year I Semester Examinations Computer Networks

(Electronics Communication and Engineering)

Time: 3hours Max Marks: 70 Note: This question paper contains two questions from each of five Units. Answer any one full question from each unit. Each question carries 14 marks and may have a, b, c as sub questions. 1. Explain TCP/IP Protocol Suit with neat sketch and list out differences between TCP/IP and OSI model (14M)(OR) 2. Write short notes on internet. (14M)3. a) Explain about services provided by PPP and also list out the services that are not provided by (7M)b) Explain Pure and derive expression for its throughput. (7M)(OR) 4. a) Explain about different strategies that are employed under controlled access. (6M)b) Explain in detail about working of TDMA and also list out differences between TDMA, FDMA and CDMA. (8M)5. a) Write short notes on giga bit ethernet. (14M)b) Explain in detail about hidden and exposed node problems in wireless lans (OR) 6. What do you mean by virtual lan and explain in detail about configuring and maintaing data of virtual lans. (7M)With the aid of suitable example explain about frequency reuse principle. (7M)7. a) Explain in detail about IGMP. (7M)b) Is multicast routing is same as multiple unicast routing, Explain. And also write short notes on MOSPF (7M)(OR) 8. a) Explain Transport layer Connection Establishment and Connection Release. (7M)b) Explain Transport protocol addressing. (7M)

a) Explain TCP header format.		(7M)
b) Explain TCP Congestion Control.		(7M)
	(OR)	
Explain the following		
a) SMTP		(7M)
b) HTTP		(7M)
	b) Explain TCP Congestion Control. Explain the following a) SMTP	b) Explain TCP Congestion Control. (OR) Explain the following a) SMTP

Time: 3hours

MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY (Autonomous Institution – UGC, Govt. of India)

B. Tech IV Year I Semester Examinations Computer Networks

Max Marks: 70

(Electronics Communication and Engineering)

Note: This question paper contains **two questions from each of** five Units. Answer **any one full** question from each unit. Each question carries 14 marks and may have a. b. c as sub questions.

ch unit. Each question carries 14 marks and may have a, b, c as sub questions.	
 a) Explain in detail about layering scenario. b) Write short notes on different levels of addressing mechanism employed in internet (OR) Explain different kinds transmission media used for internet. 	(6M) (8M) (14M)
 3. a) Explain error detection using CRC for the following. Consider a message 110010 represented by the polynomial M(x) = x5 + x4 + x and a generating polynomial G(x) = x3 + x2 + 1 (1101) b) Explain in detail about different fields present in PPP frame format. (OR) 4. a) Draw and explain HDLC frame format and also explain about different types of frames used in HDLC. b) Explain how slotted aloha improves the performance of pure aloha 	(7M) (7M) (8M) (7M)
 5. a) Discuss briefly about the MAC layers in the 802.11 standard. b) Explain in detail about the Physical layer in the Fast Ethernet (OR) 6. a) Describe in detail about the Frequency Division Multiple Access. b) What is learning bridge and explain in detail about the process of learning of learning bridge 	(14M) (14M) (7M)
 7. a) Write short notes on IPV6 addresses. b) Explain indetail about message format and different types of error reporting messages of ICMP. (OR) 8. With a suitable example explain Distance Vector Routing algorithm. What is the serious drawback of Distance Vector Routing algorithm? Explain. 	(7M) (7M) (14M)

9.	a) Explain TCP header format.	(7M)
	b) What is WEB Documents? Explain with its categories.	(7M)
	(OR)	
10.	a)Write short notes on SMTP	(7M)
	b) Write short notes of different techniques that are employed to improve QoS	(7M)

MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY (Autonomous Institution – UGC, Govt. of India)

B. Tech IV Year I Semester Examinations Computer Networks

(Electronics Communication and Engineering)

Time: 3hours Max Marks: 70 Note: This question paper contains two questions from each of five Units. Answer any one full question from each unit. Each question carries 14 marks and may have a, b, c as sub questions. 1. a) Explain in detail about layering scenario. (6M)b) Write short notes on different levels of addressing mechanism employed in internet (8M)(OR) 2. Explain different kinds transmission media used for internet. (14M)3. a) Given 1101011011 data frame and generator polynomial G(x) = x4 + x + 1. Derive the transmitted frame (7M)b) Explain in detail about CSMA/CA. (7M)(OR) 4. a) Explain in detail about CSMS/CD (8M)b) Give a brief note on the Multilink Point to point protocol (7M)5. a) Why there is no need for CSMA/CD on a full-duplex Ethernet LAN? Explain. (14M)b) Write short on back bone networks (OR) 6. a) Describe in detail about the CDMA. (7M)b) Write short notes on IEEE 802.11 (7M)7. a) Explain briefly about the shortest path routing algorithm. (6M)b) Explain indetail about classfull addressing and classless addressing. (8M)8. a) What is Count to infinity problem? Explain with suitable example. (7M)b) Write short notes on internetworking (7M)

between SCTP and TCP. (7M)
b) Write short notes of different techniques that are employed to improve QoS (7M)
(OR)

10. a) List out the different fields that are missing in TCP header as compared to that of UDP and give the reasons for their missing. (7M)

(7M)

b) What is WEB Documents? Explain with its categories.

9. a) Draw frame format of SCTP and discuss indetail about each field. Also list out differences



R13

[10]

Code No: 117BY

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, November/December - 2016 COMPUTER NETWORKS (Common to ECE PAGE)

	(Common to ECE, BALE)	
Time:	3 Hours	Max. Marks: 75
Note:	This question paper contains two parts A and B.	
	Part A is compulsory which carries 25 marks. Answer all ques	tions in Part A
	Part B consists of 5 Units. Answer any one full question	from each unit
	Each question carries 10 marks and may have a, b, c as sub questions.	wom cuen unit.

PART- A

	PART- A	
		(25 Marks)
1.a) Write short notes on interfaces.	[2]
b	e de la companya de	[3]
C		[2]
d	· · · · · · · · · · · · · · · · · · ·	[3]
e		[2]
f	Difference between connectionless and connection oriented networks.	[3]
7) Explain about CIDR.	[2]
g h) Explain the functions of Transport layer.	[3]
ī	Explain about TELNET.	[2]
i) j)	Write the application layer paradigms.	[2] [3]
	PART-B	
		(50 Marks)
2.a) b)	Explain the functions of various layers in ISO-OSI reference model. Explain the term sliding window. Also illustrate and explain the operation repeat.	of selective
	OR	L1
3.a)	Discuss about unguided transmission media.	
b)	What are the different types of error detection methods? Explain the CRC ex	mor detection
-7	technique using generator polynomial x^4+x^3+1 and data 11100011.	[5+5]
4.a)	Explain the operation of source Routing Bridges.	
b)	Explain the working of CSMA/CD.	[5+5]
	OR	
5.a)	Discuss in brief the MAC frame structure for IEEE 802.3	
b)	Explain in detail the operation of pure ALOHA and slotted ALOHA.	[5+5]
6.a)	Explain the Dijkstra's Shortest Path Routing Algorithm with an example.	
b)	Give the general principles of various congestion control algorithm. OR	[5+5]
7.	What is Congestion control? How it is implemented in Network Layer? What	is the role of

Choke packet in managing congestion?

a.aj	Explain the error control mechanism in dansport layer.	
b)	Explain about Reverse Address Resolution Protocol.	[5+5]
•	OR	
9.a)	How are connection establishment and connection release managed at the tr Explain.	ansport layer?
b)	With a neat diagram explain the IPv6 header format.	[5+5]
10.a)	Compare and Contrast the UDP header and the TCP header.	
b)	Explain the client server model.	[5+5]
	OR	
	What is Electronic mail? Explain the two scenarios of architecture of E-Mail. Explain the TCP service model.	[5+5]

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Code No: 117BY

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech IV Year 1Semester Examinations, November/December - 2017 COMPUTER NETWORKS

(Common to ECE, EIE, BME)

Time:	3 Hours	Max. Marks: 75
Note:	This question paper contains two parts A and B.	
	Part A is compulsory which carries 25 marks. Answer all question	ns in Part A. Part B
	consists of 5 Units. Answer any one full question from each u	
	carries 10 marks and may have a, b, c as sub questions.	
	Part- A	
		(25 Marks)
1.a)	What is CRC checker?	[2]
b)	Write the advantages of layered architecture of network.	[3]
c)	Define exponential Back off.	[2]
d)	What is piggy backing? How does it useful?	[3]
e)	Write the functions of LLC.	[2]
f)	Write the responsibilities of network layer.	[3]
g)	What is multiplexing? Give different types of multiplexing?	[2]
h)	Write about Tunneling.	[3]
i)	What is DNS? Write its properties.	[2]
j)	Explain MIME header	[3]
	Part-B	
	Tart-D	(50 Marks)
		(50 Marks)
2.a)	Compare TCP/IP and OSI reference model.	
b)	Explain about framing.	[5+5]
	OR	
3.a)	Explain stop and wait protocol,	
b)	Give a detail note on Hamming code.	[5+5]
4.a)	Explain CSMA/CD protocol and how does it detect collision?	
b)	Discuss about switched and fast Ethernet.	[5+5]
	OR	
5.a)	Explain MAC sub layer protocol in detail.	
b)	Discuss about spanning tree bridges.	[5+5]
6.a)	Explain link state routing algorithm in detail.	
b)	Write the optimality principle of routing algorithms.	[5+5]
7-1	OR	
7.a)	Describe hierarchical routing algorithm in detail.	[6+6]
b)	Write a note on load shedding.	[5+5]

8.a)	Explain IPV6 packet format.	
b)	Describe fragmentation in internet working with an example.	[5+5]
	OR	
9.a)	Explain Address resolution protocol in detail.	
b)	Write the principles of network layer in internet.	[5+5]
10.a)	Explain TCP sliding window protocol.	
b)	Give a detail note on HTTP request-response model.	[5+5]
	OR	
11.a)	Explain File transport protocol.	
b)	Compare TCP and UDP protocols.	[5+5]

Code No: 117BY

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech IV Year I Semester Examinations, March - 2017 COMPUTER NETWORKS

(Common to ECE_FIF_RMF)

		(Common to ECE, EIE, BME)		Man Manka 75	
		3 Hours This question names contains two parts A and B		Max. Marks: 75	
	Note:	This question paper contains two parts A and B. Part A is compulsory which carries 25 marks. Answer consists of 5 Units. Answer any one full question from e 10 marks and may have a, b, c as sub questions.	all questions ach unit. Eac	in Part A. Part B h question carries	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
		Part- A (25 Marks)			
	1.a)	How selective repeat protocol resolves issues of stop and	wait protocol?	[2]	
***	b)	What are the applications of Infrared waves?		:[3]···: :[2]···:	
***	: : e)	Mention some of the physical properties of Ethernet. Explain the function of repeaters.		[3]	, ,
	e)	What are the metrics used by routing protocols.		[2]	
	f)	How does netid differ from a network address.		[3]	
	g)	Explain briefly about Crash recovery.	1 1.**	[2]	1. 11 v***
	h)	Explain about Packet Fragmentation. What are the basic functions of email systems?		[3]	Mod
$\overline{}$	j)	What are the two main categories of DNS messages?		[3]	
		Part-B (50 Marks)			
A. T.	-2.a)	Explain about the Coaxial Cable with next sketch.			k.i C
	b)	What is bit and byte stuffing explain with an example.	1 1,444	[5+5]	1 1744
	3.a)	OR Explain the frame format of PPP.			
	b)	Draw the layered architecture of the OSI reference	model and v	write two service	S
	: 1	provided by each layer of the model.		[5+5]	1. 1.00
		8 8 818			1 11
	4.a) b)	Explain the flow diagram of CSMA/CD. Explain about the source routing bridge.		[5+5]	
		OR			
	5.a)	Explain about channelization protocols.		[5+5]	
	b)	Explain the categories of standard Ethernet.		[5+5]	
")	6.	Explain about the Distance Vector routing protocol with	an example.	[10]	
	7.	OR Explain about the Link State routing algorithm.		[10]	
·***:	8	Explain about DHCP.		[10]	1
		OR		1 1 1	1 14.
	9.a) b)	Explain about CIDR. Explain about RARP.		[5+5]	
	10.	Explain the various fields of the TCP header with the he	elp of a neat di	agram.[10]	
1111	- 1 - 1	OR C		1 1 2 1 1 1	
****	11:a) b)	Explain about the window management in TCP. Explain about HTTP request.		[5+5]	

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech IV Year I Semester Examinations, June/July- 2014

COMPUTER NETWORKS

(Common to ECE, EIE, BME, ECM)

Time: 3 Hours

Max. Marks: 75

Answer any Five Questions All Questions Carry Equal Marks

Write any four reasons for using layered protocols.

- Explain the functionality of each layer in OSI reference model.
- 2.a) If the bit string 0111101111101111110 is bit stuffed. What is the output of the string?
 - b) What is the reminder obtained by dividing x⁷+x⁵+1 by the generator x³+1?
- With an example, explain the importance of sequence number for Acknowledgements.
 - Explain stop-and-wait protocol.
- 4. What is a token? Discuss the protocol of token ring LAN in general. Explain with an example how priority is implemented in a token ring LAN?
- 5.a) Describe design goals, architecture and switching mechanisms of ATM networks.
- Explain the functions of following devices:
 - i) Hub
- ii) Bridge
- iii) Router
- iv) Gateway.
- 6.a) The major problem with distance vector algorithm is 'count to infinity'. How exchange of complete path from router to destination instead of delay, helps in solving count to infinity problem.
 - b) What are the advantages of adaptive routing approach over non adaptive routing?
- Write short notes on:
 - a) Admission control
 - b) Choke packet
 - c) Load shedding
 - d) Jitter control.
- What is DNS? Explain its usage and its working?



III B. Tech II Semester Regular Examinations, Feb-2018 COMPUTER NETWORKS

(Common to CSE and IT)

Tir	ne: 3	(Common to CSE and IT) 3 hours N	/ax. Marks: 70
		Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answering the question in Part-A is compulsory 3. Answer any THREE Questions from Part-B *****	
		PART -A	
1	a)	Write about connection oriented service-reliable communication	[4M]
	b)	Explain circuit switching technology implementation in Telephone networks	i. [3M]
	c)	With suitable example explain internet checksum.	[4M]
	d)	How to route the packets in virtual circuit subnets?	[4M]
	e)	Describe various access methods in standard Ethernet.	[4M]
	f)	What is URL? How it will be processed? Explain.	[3M]
		PART -B	
2	a)	Give the structure and working principle of WAN with virtual private networks and Internet Service Provider. And also explain its role in Internet.	[8M]
	b)	Write about peer-to-peer processes and encapsulation concepts in OSI model	
3	a)	Describe the functional differences between statistical and synchronous time division multiplexing.	[8M]
	b)	With four switches draw the architecture of datagram networks and explain the data transfer between nodes.	[8M]
4	a)	Show the generation of codeword at the sender site and check the same at the	:
		receiver site using CRC where data word is 1010011010 and the deviser is 10111.	[8M]
	b)	"In Selective Repeat ARQ, the size of the sender and receiver window must be at most one-half of 2 ^m justify the statement.	[8M]
5	a)	With example explain routing process in hierarchical routing.	[8M]
	b)	Explain all variations of "sense before transmit" methods used in multiple access.	[8M]
6	a)	What are the addressing mechanisms followed in IEEE802.11. How it solves hidden station and exposed station problem.	[8M]
	b)	Explain the MAC sub layer and physical layer specifications in high speed LAN.	[8M]
7		Explain the following with respect to HTTP	
	a	Operational Model	[6M]
	b	Request message format	[5M]
	c	Reply message format.	[5M]

III B. Tech II Semester Regular Examinations, Feb-2018 COMPUTER NETWORKS

(Common to CSE and IT)

ege.c		(Common to CSE and 11)	
Tii	ne: 3		Max. Marks: 70
		Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answering the question in Part-A is compulsory 3. Answer any THREE Questions from Part-B *****	
		PART-A	
1	a)	Write the characteristics of Wide Area Networks.	[3M]
	b)	What are the design issues of physical layer?	[4M]
	c)	Differentiate the process of error correction and error detection in block coding.	[4M]
	d)	Write about the vulnerable time period in slotted ALOHA protocol.	[4M]
	e)	With an example explain variations of Manchester encoding.	[4M]
	f)	Explain the architecture of browser-server.	[3M]
		PART -B	
2	a)	Differentiate services, mechanisms and interfaces with respect to OSI and TCP/IP protocol suits.	[8M]
	b)	What is network hardware? Explain in detail with respect to transmission technology and scale of networks.	[8M]
3	a)	What is the difference between the routing process in datagram networks an in virtual circuit networks? Explain	d [8M]
	b)	Write about the multiplexing and de-multiplexing process in frequency division multiplexing	[8M]
4	a)	What is sliding window? How it is used in noisy channels for error control.	[8M]
	b)	Write the sender site and receiver site algorithm for simplest protocol and st and wait protocols.	[RM]
5	a)	Explain the optimality principle with respect to shortest path algorithm	[8M]
	b)	What is channelization? Explain any two channelization techniques.	[8M]
6	a)	Describe the architecture and physical layer specifications of f IEEE802.11 standard.	[8M]
	b)	Write the differences between bridged Ethernet, switched Ethernet and full duplex Ethernet.	[8M]
7	a)	In detail write about WAP protocol implementation for wireless Web.	[8M]
	b)	With neat sketch explain the formats of generic messages in HTTP. How security is provided for HTTP messages.	[8M]

Code No: RT32053 (R13) (SET - 3)

III B. Tech II Semester Regular Examinations, Feb-2018 COMPUTER NETWORKS

(Comm to CSE and IT)

		(Comm to CSE and II)			
Tir	me: 3	hours M	lах.	Marks: 70	
		Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answering the question in Part-A is compulsory 3. Answer any THREE Questions from Part-B *****			
		PART-A			
1	a)	Write about the original ARPANET design.		[3M]	
	b)	Write short notes on frame synchronization in TDM.		[4M]	
	c)	Differentiate character oriented and bit oriented protocols.		[4M]	
	d)	Write a short notes on persistence methods		[4M]	
	c)	Discuss the addressing mechanisms of wireless LANs.		[4M]	
	f)	What is proxy server? How it is related to HTTP.		[3M]	
		PART -B			
2	a)	Differentiate the following with respect to OSI Layers functionality i) Logical Address ii) Physical Address iii) Service Point address		[8M]	
	b)	Describe different types of networks we encounter in the world today. And a differentiate point-to-point WAN and switched WAN.	lso	[8M]	
3	a)	What are different multiplexing techniques used for analog signals? Explain.		[8M]	
	b)	Write the characteristics of virtual circuit networks and explain source to destination data transfer in it.		[8M]	
4	a)	Show that the maximum window size in selective repeat is 2 ⁿ /2 and go-back- is 2 ⁿ -1, where n is the number of bits used for fame sequence number.	n	[8M]	
	b)	How to determine the type of the frame in HDLC protocol? Explain with frame format.	ne	[8M]	
5	a)	What is random access? Explain how it can be achieved with pure ALOHA and slotted ALOHA.		[8M]	
	b)	How to solve the problem of gigantic forwarding tables? Propose and explain some routing algorithms.	1	[8M]	
6	a)	Explain frame format, addressing mechanisms and access methods in standar Ethernet.	d	[8M]	
	b)	How to use handshaking mechanism to prevent hidden station and exposed station problem, Explain,		[8M]	
7	a)	Differentiate static, dynamic and active documents used in World Wide Web		[8M]	
	b)	Explain various status codes used in HTTP protocol.		[8M]	

III B. Tech II Semester Regular Examinations, Feb-2018 COMPUTER NETWORKS

(Comm to CSE and IT)

		(Comm to CSE and IT)	
Tir	ne: 3	hours 1	Max. Marks: 70
		Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answering the question in Part-A is compulsory 3. Answer any THREE Questions from Part-B *****	
		PART-A	
1	a)	Describe store and forward networks.	[3M]
	b)	What is the role of routing table in datagram networks?	[4M]
	c)	How to achieve flow control and error control in data link layer.	[4M]
	d)	What is the role of coding theory in code division multiplexing technique?	[4M]
	c)	Differentiate basic service set and extended service set.	[4M]
	f)	Write about various components of URL.	[3M]
		PART -B	
2	a)	With neat sketch discuss the functionalities of each layer in TCP/IP protocol	
	L	suite.	[8M]
	b)	Write short notes on the Novel Netware architecture. How it helps in interne evolution?	t [8M]
3	a)	What is virtual circuit identifier? How it is used in setup and tear down phas Explain with suitable example.	es. [8M]
	b)	Explain how wavelength division multiplexing works. What are its advantage over other methods?	ges [8M]
4	a)	Explain the design and implementation of stop and wait protocol.	[8M]
	b)	Write about services, framing and multiplexing concepts of Point-Point Protocol.	[8M]
5	a)	Discuss the following: i) Broadcast Routing ii) Multicast Routing.	[8M]
	b)	What is multiple access control? Explain various protocols used to impleme this.	nt [8M]
6	a)	Describe the architecture, MAC sub layer, addressing mechanisms of wirele LANs	ss [8M]
	b)	Write the physical layer specifications of fast Ethernet, How they are differe from standard Ethernet,	nt [8M]
7	a)	Describe the operational model of HTTP protocol, Relate this with WWW a FTP.	nd [8M]
	b)	How to access information over a mobile through WAP? Explain its protoco	l [8M]

design.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

IV ECE (R15-AUTONOMOUS)

EMBEDDED SYSTEM DESIGN MODEL QUESTION PAPERS

MODEL QUESTION PAPER-1

Code No: A70440

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY B.Tech. IV Year - I Semester Examinations EMBEDDED SYSTEM DESIGN

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

	PART -A	(25 Marks)
1.	a) What are large scale embedded systems	[2M]
	b) What are data collection/storage embedded systems	[3M]
	c) What is the difference between RISC and CISC	[2M]
	d) What is a digital signal processor	[3M]
	e) What is firmware	[2M]
	f) What is a linker	[3M]
	g) What is kernel	[2M]
	h) Explain difference between preemptive and non preemptiv	e scheduling
		[3M]
	i) What is inter process communication	[2M]
	j) What is task synchronization	[3M]

PART-B (50 Marks)

SECTION-I

2) Explain about significance of embedded system and classification of the $\ [10M]$ Embedded systems.

(OR)

3) Explain the purpose of embedded systems.

SECTION-II

4) Explain the elements of the embedded system with neat sketch [10M](OR)5) Explain about ASICs, PLDs and COTs.

SECTION-III

- 6) Explain the significance of reset circuit and brownout protection circuit. [10M] (OR)
- 7) Explain about firmware design approaches

SECTION-IV

- 8) Explain about process and the process states with neat sketch \$[10M]\$ (OR)
- 9) Explain the non preemptive FCFS algorithm with an example

SECTION-V

- 11) Explain how shared data problems can be overcome with task synchronization Techniques

MODEL QUESTION PAPER-2

Code No: A70440

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY B.Tech. IV Year - I Semester Examinations EMBEDDED SYSTEM DESIGN

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART - A (2)	5 Marks)
1. a) What is embedded system	[2M]
b) What is product life cycle curve	[3M]
c) What is the difference between Little Endian and Big Endiannes	ss. [2M]
d) What is the difference between SRAM and DRAM	[3M]
e) What is super loop approach	[2M]
f) What is Hex file	[3M]
g) What are the types of Multitasking	[2M]
h) What are the factors for scheduling	[3M]
i) What are memory mapped objects	[2M]
j) What is deadlock and starvation	[3M]

Part-B (50 Marks)

SECTION-I

2). Explain the difference between Embedded Systems and General [10M]

Computing Systems

(OR)

3). Explain the characteristics of embedded systems

SECTION-II

4). Explain about core of the embedded system [10M] (OR) 5). Explain about the I2C protocol with neat sketch **SECTION-III** 6). Explain the Real Time Clock (RTC) and Watchdog timer. [10M] (OR) 7). Explain the advantages and disadvantages of using the assembly language for firmware design. [10M] **SECTION-IV** 8). Explain about hard real time system and soft real time system with an example [10M] (OR) 9). Explain the functions of real time kernel **SECTION-V** 10). Explain about message queues and mail boxes with neat sketch [10M] (OR)

11). Explain about rat race condition, deadlock, starvation with an example

MODEL QUESTION PAPER-3

Code No: A70440

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY B.Tech. IV Year - I Semester Examinations EMBEDDED SYSTEM DESIGN

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART -A	(50 Marks)
1. a)What are the applications of embedded systems	[2M]
b) What are the data processing and monitoring systems	[3M]
c) What is commercial off the shelf component	[2M]
d) What is UART	[3M]
e) What is locator	[2M]
f) What are onboard communication interfaces	[2M]
g) What is multi threading	[3M]
h) What is Roundrobin algorithm	[3M]
i) What is a Socket	[2M]
j) What is a binary semaphore	[3M]
PART-B	(50 Marks)
SECTION-I	
2) Explain the major application areas of embedded systems	[10M]
(or)	

3) Explain about operational quality attributes of embedded system

SECTION-II

4) Explain about different types of memory used in embedded system applications [10M]

(or)

5) Explain the operation of optocoupler and relay

SECTION-III

6) Explain about memory shadowing technique and the memory selection for embedded systems [10M]

(or)

7) Explain about assembly language to machine language development process with neat sketch

SECTION-IV

8) Explain about process, process structure and memory organization of process [10M]

(or)

9) Three processes with process ids p1, p2,p3 with estimated completion time 10,5,7 milliseconds respectively enters the ready queue together. Calculate the waiting time, average waiting time, turnaround time and average turnaround time in SJF algorithm

SECTION-V

10) Explain the dining philosopher's problem with different scenarios [10M]

(or)

11) Explain how semaphores are used for task synchronization

MODEL QUESTION PAPER-4

Code No: A70440

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY B.Tech. IV Year - I Semester Examinations EMBEDDED SYSTEM DESIGN

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART -A	(25 Marks)
1. a) What is testability and debug-ability	[3M]
b) What is throughput	[2M]
c) What is the difference between Von Neumann archited	ture and Harvard
architecture	[3M]
d) What is seven segment display	[2M]
e) What is flash memory	[2M]
f) What are the processes states	[3M]
g) What is turnaround time	[2M]
h) What is context switching	[3M]
i) What is mail box	[2M]
j) What are POSIX threads	[3M]
PART -B	(50 Marks)
SECTION-I	
2) Explain about embedded system with an example	[10M]
(or)	

3) Explain about non-operational quality attributes of embedded system

SECTION-II

4) Explain about SPI and 1 wire interface bus

[10M]

(or)

5) Explain about Wifi and Zigbee external communication interfaces

SECTION-III

6) Explain about the high level language development process

[10M]

(or)

7) Explain about mixing assembly language with high level language

SECTION-IV

8) Explain about multitasking, multi processing and multithreading concepts[10M]

(or)

9) Three processes with process ids p1, p2,p3 with estimated completion time 8,2,6 milliseconds respectively enters the ready queue together in the order p1,p2,p3.calculate the waiting time, average waiting time, turnaround time, average turnaround time in round robin algorithm with time slice =2ms

SECTION-V

10) Explain the producer consumer bounded buffer problem with an example [10M]

(or)

11) Explain the priority inversion problem and explain any one of the priority inversion workarounds

MODEL QUESTION PAPER-5

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY B.Tech. IV Year - I Semester Examinations EMBEDDED SYSTEM DESIGN

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B

2)

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART -A (25 Marks)

1. a) What is general purpose system	[2M]
b) What is mean time between failure and mean time to repair	terms[3M]
c) What is the difference between microprocessor and ASIC	[3M]
d) What are sensors and actuators	[2M]
e) What is hard real time system	[3M]
f) What is the difference between GPOS and RTOS	[2M]
g) What are the functions of kernel	[2M]
h) What is the need of task communication	[3M]
i) What is the need of task synchronization	[2M]
j) What is task/process scheduling	[3M]
PART -B	(50 Marks)
SECTION-I	
Explain about classification of embedded systems	[10M]
(or)	

3) Explain about operational and non operational attributes of the embedded system

SECTION-II

4) Explain about INFRARED and RS-232 communication interfaces

[10M]

(or)

5) Explain about USB and Bluetooth external communication interfaces

SECTION-III

6) Explain about the high level language development process

[10M]

(or)

7) Explain the advantages and limitations of the high level language based development

SECTION-IV

8) a) Differentiate GPOS and RTOS

[10M]

b) Differentiate microkernel and monolithic kernel

(or)

9) Three processes with process ids p1, p2,p3 with estimated completion time 10,5,7 milliseconds and priorities 1, 3,2 respectively enters the ready queue together. A new process p4 with estimated completion time 6ms and priority 0 enters the ready queue after 5ms of the start of execution of p1. in the order p1,p2,p3.calculate the waiting time, average waiting time, turnaround time, average turnaround time in preemptive priority scheduling algorithm

SECTION-V

10) Explain the task communication techniques

[10M]

(or)

11) Explain about semaphores and events

IV B.Tech I Semester Supplementary Examinations, February/March - 2018 DIGITAL IMAGE PROCESSING

(Common to Electronics and Computer Engineering, Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

PART-A (22 Marks)

1.	a)	Define the following terms:	
		(i) Image (ii) Resolution (iii) Pixel and (iv) Digital Image	[4]
	b)	Compare Image Enhancement and Image Restoration.	[4]
	c)	Give the relation for degradation model for Continuous function.	[3]
	d)	Differentiate Pseudo color image processing and full color image processing.	[4]
	e)	What is the need for Compression?	[4]
	f)	What are the applications of Image segmentation?	[3]
		$\underline{\mathbf{PART-B}}\ (3x16 = 48\ Marks)$	
2.	a)	Compute Haar Transform for following N Value. N=8.	[8]
	b)	Explain how Fourier transforms are useful in digital image processing and	FO.
		explain the properties of Fourier transform.	[8]
3.	a)	Define Histogram of Image. Explain the concept of Histogram Equalization	
		technique for Image enhancement.	[8]
	b)	Explain Spatial filtering in Image enhancement.	[8]
4.	a)	Explain the need for Image restoration.	[8]
	b)	Explain the concept of Inverse Filtering and also mention the limitations of it.	[8]
5.	a)	Explain about color segmentation process.	[8]
٠.	b)	Discuss the procedure for conversion from RGB color model to HSI color model.	[8]
	,		
6.	a)	Draw and explain the general image compression system model.	[8]
	b)	Write short notes on Image Pyramids and Sub band coding.	[8]
7.	a)	Explain the significance of thresholding in image segmentation.	[8]
	b)	Write short notes on some basic morphology algorithms.	[8]

R13

Code No: **RT41043**

Set No. 1

[2]

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 **DIGITAL IMAGE PROCESSING**

(Common to Electronics and Computer Engineering, Electronics and Communication **Engineering and Electronics and Instrumentation Engineering)**

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B ****

PART-A (22 Marks)

1.	a)	Define D ₄ and D ₈ distances.	$[\mathfrak{I}]$
	b)	What are the advantages of filtering in frequency domain?	[4]
	c)	How to estimate the degradation function by experimentation?	[4]
	d)	Define brightness, hue and saturation.	[3]
	e)	Write short notes on spatial redundancy.	[4]
	f)	Write short notes on morphological gradient.	[4]
		PART-B (3x16 = 48 Marks)	
2.	a)	What is meant by image interpolation? Discuss about various interpolation	
		methods.	[8]
	b)	What is the need of image transform? List out various transform used in image	
		processing.	[8]
3.	۵)	With an axample axalain the concent of histogram equalization	го 1
٥.	a)	With an example, explain the concept of histogram equalization.	[8]
	b)	State 2D sampling theorem and explain about aliasing in images.	[8]
4.	a)	Explain about noise reduction in an image using band reject and band pass filters.	[8]
	b)	Explain the concept of minimum mean square error filtering.	[8]
5.	a)	Explain about RGB color model and write its applications.	[8]
	b)	Describe about histogram processing in color images.	[8]
6.	a)	Draw the diagram of two band subband coding and decoding system, and explain	
		it.	[8]
	b)	With an example, explain about arithmetic coding.	[8]
	•		
7.	a)	Discuss about opening and closing for gray scale images.	[8]
	b)	Explain the detection of isolated points in an image.	[8]

R13

Code No: **RT41043**

Set No. 2

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 DIGITAL IMAGE PROCESSING

(Common to Electronics and Computer Engineering, Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

1.	a)b)c)d)e)f)	PART-A (22 Marks) What is meant by spatial resolution and explain its significance. Define Fourier spectrum and Phase angle of 2D-DFT. Write short notes on Max and Min filters. Write short notes on chromaticity and tristimulus values. Explain about subjective fidelity criteria. Explain the duality of erosion and dilation operations.	[4] [3] [4] [4] [3] [4]
		$\underline{\mathbf{PART-B}} \ (3x16 = 48 \ Marks)$	
2.	a)b)	Explain the following terms: (i) Adjacency (ii) Connectivity (iii) Regions (iv) Boundaries Obtain the Haar transformation matrix for N = 8.	[8] [8]
3.	a) b)	Explain the use of histogram statistics for image enhancement. Prove the validity of the discrete convolution theorem of two variables.	[8] [8]
4.	a) b)	What is an adaptive median filter? Explain its use for noise reduction in an image. With an example, explain the concept of image reconstruction from back	[8]
		projections.	[8]
5.	a) b)	Discuss about CMY and CMYK color models. Discuss about noise in color images.	[8] [8]
6.	a)	Explain the concept of wavelet packets and write its advantages.	[8]
	b)	Draw the functional block diagram of general image compression system and explain it.	[8]
7.	a) b)	Explain the following morphological algorithms: (i) Boundary extraction (ii) Hole filling Define image gradient and explain its use in edge detection.	[8] [8]

1 of 1

[4]

[3]

[8]

[8]

[8]

[8]

[8]

IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 DIGITAL IMAGE PROCESSING

(Common to Electronics and Computer Engineering, Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****

PART-A (22 Marks)

- 1. a) Compute the Haar transform of the 2 X 2 image $F = \begin{bmatrix} 3 & -1 \\ 6 & 2 \end{bmatrix}$ [4]
 - b) What is Log Transformation and write its use in image processing. [3]
 - c) Write the expression for contraharmonic mean filter and explain its use in image restoration.
 - d) What is the purpose of color model and list out some color models. [4]
 - e) What is image compression? Why it is needed? [4]
 - f) List out different masks used to compute the gradient.

PART–B (3x16 = 48 Marks)

- 2. a) Explain the basic concepts of sampling and quantization in the generation of digital image. [8]
 - b) Discuss about KL Transform and write its applications in image processing. [8]
- 3. a) Determine the convolution and correlation between the following images:

- b) Explain the following filters:
 - (i) Band reject and Band pass filters (ii) Notch filters
- 4. a) What are the different approaches to estimate the noise parameters in an image? Explain.
 - b) State and explain the Fourier-Slice Theorem. [8]
- 5. a) Discuss the concept of converting colors from RGB to HSI.
 - b) With necessary equations, explain about color edge detection.
- 6. a) What are the various Multiresolution analysis requirements? Explain. [8]
 - b) What is meant by block transform coding? Explain. [8]
- 7. a) Explain about morphological hit-or-miss transform. [8]
 - b) Discuss about edge linking using local processing. [8]

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IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017 DIGITAL IMAGE PROCESSING

(Common to Electronics and Computer Engineering, Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

PART-A (22 Marks)

1.	a)	Define Walsh Transform and write its properties.	[4]
	b)	What is meant by gamma correction? Why it is needed?	[3]
	c)	Write the difference between image restoration and image enhancement.	[4]
	d)	Write short notes on RGB to CMY conversion.	[4]
	e)	Write the difference between Fourier transform and wavelet transform.	[4]
	f)	Explain the effect of noise in edge detection.	[3]
		$\underline{\mathbf{PART-B}} \ (3x16 = 48 \ Marks)$	
2.	a)	Explain about linear and nonlinear operations used in image processing.	[8]
	b)	State and Prove the translation and rotation properties of 2D-DFT.	[8]
3.	a)	Explain the concept of weighted average filter.	[8]
	b)	With necessary equations, explain the concept of homomorphic filtering.	[8]
4.	a)	List out some important noise probability density functions used in image	
		processing and sketch their plots.	[8]
	b)	Discuss about Radon Transform and write its applications.	[8]
5.	a)	Explain about intensity slicing and write its applications.	[8]
	b)	Discuss about segmentation in RGB vector space.	[8]
6.	a)	Explain about wavelet transform in two dimensions.	[8]
	b)	Draw the block diagram of lossless predictive coding model and explain it.	[8]
7.	a)	Explain the following morphological operations:	
		(i) Erosion	
		(ii) Dilation	[8]
	b)	Explain the basics of intensity thresholding in image segmentation.	[8]

IV B.Tech I Semester Supplementary Examinations, March - 2017

DIGITAL IMAGE PROCESSING

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B

PART-A (22 Marks)

1.	a)	Describe Weber ratio.	[4]
	b)	Illustrate first and second derivatives of a 1-D digital function representing a	
		section of horizontal intensity profile from an image.	[4]
	c)	Explain about Arithmetic mean filter.	[4]
	d)	Discuss about Tonal correction.	[4]
	e)	Write a short note on Compression Ratio.	[4]
	f)	What is global, Local and dynamic or adaptive threshold?	[2]
		$\underline{PART-B} (3x16 = 48 Marks)$	
2.	a)	Explain Fast Fourier Transform (FFT) in detail.	[8]
	b)	Describe image formation in the eye with brightness adaptation and	
		discrimination.	[8]
3.	a)	What effect would setting to zero the half of lower-order bit planes have on the	
٥.	u)	histogram of an image in general.	[8]
	b)	Discuss the limiting effect of repeatedly applying a 3x3 low-pass spatial filter to a	L-3
		digital image. You may ignore border effects. Is this effect different from applying	
		5x5 filter?	[8]
4.	a)	What are the two approaches for blind image restoration? Explain in detail.	[8]
	b)	Explain about interactive image restoration.	[8]
	0)	2p.u.m ucout micrueti ve miuge restoruizon.	[0]
5.	a)	Briefly discuss about Complements on the color circle.	[8]
	b)	What is color image smoothing? Explain how smoothing will done by	
		neighborhood averaging.	[8]
6.	a)	Explain about the Fast Wavelet Transform.	[12]
	b)	Write a short note on Wavelet Packets.	[4]
	0)	THE a short hote on Travelet I across.	[ד]
7.	a)	How can you control Over segmentation problem? Explain it.	[8]
	b)	Write short notes on Haar Transforms.	[8]

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IV B.Tech I Semester Regular Examinations, November - 2016 DIGITAL IMAGE PROCESSING

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****

PART-A (22 Marks)

1.	a)	Define neighbors of a pixel.	[3]
	b)	Write short notes on selective filtering.	[4]
	c)	Write the difference between image restoration and image enhancement.	[4]
	d)	What is the advantage of color in image processing applications?	[4]
	e)	What is meant by digital image water marking?	[3]
	f)	What is meant by image segmentation? Write its use in image processing.	[4]
		$\underline{\mathbf{PART-B}} (3x16 = 48 \ Marks)$	
2.	a)	Explain the following mathematical operations on digital images	
	b)	i) Array versus Matrix operations ii) Linear versus Nonlinear Operations Explain the following two properties of 2D-DFT:	[8]
	٥,	i) Convolution ii) Correlation	[8]
3.	a)	What is meant by histogram specification? Explain.	[8]
	b)	Explain image smoothing using ideal lowpass filters and Butterworth lowpass	
		filters.	[8]
4.	a)	What are the advantages of adaptive filters? Explain about adaptive median	
		filter.	[8]
	b)	Explain about image restoration using inverse filtering. Write the draw backs of	507
		this method.	[8]
5.	a)	What is Pseudocolor image processing? Explain.	[8]
	b)	Explain about color image smoothing.	[8]
6.	a)	Explain two-band subband coding and decoding system.	[8]
	b)	With an example, explain about run-length coding.	[8]
_			
7.	a)	What is Hit-or-Miss transformation? Explain.	[8]
	b)	Explain about edge detection using gradient operator.	[8]

IV B.Tech I Semester Regular Examinations, November - 2016

DIGITAL IMAGE PROCESSING

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours Max. Marks: 70 Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B **** PART-A (22 Marks) What is the need for image transform? Explain. 1. a) [4] b) What is meant by moiré patterns? Explain. [4] Draw the model of Image degradation/Restoration process. c) [3] What is the significance of color model? d) [4] Define subband coding? e) [3] f) Explain how a point can be detected in an image? [4] PART-B (3x16 = 48 Marks)Explain the various basic relationships between pixels. 2. a) [8] What is Haar Transform? Write the procedure to determine the Haar b) transformation matrix. [8] 3. a) Explain the following operations: [8] i) Contrast stretching ii) Bit-plane slicing What is notch filter? Explain its use in image processing. [8] b) List out different noise probability density functions used in image processing 4. a) applications. [8] With an example, explain how an image can be reconstructed from projections. [8] b) 5. a) Explain about RGB color model? [8] Explain about histogram processing of color images. b) [8] What are the various requirements for multi-resolution analysis? Explain. [8] 6. a) Draw the functional block diagram of image compression system and explain the b) purpose of each block. [8] Explain the following morphological algorithms 7. a) i) Boundary extraction ii) Hole filling [8] What is meant by edge linking? Explain edge linking using local processing. b) [8]

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IV B.Tech I Semester Regular Examinations, November - 2016

DIGITAL IMAGE PROCESSING

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours Max. Marks: 70 Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B **** PART-A (22 Marks) 1. a) What is meant by isopreference curves? Explain. [4] b) What is log transformation? How it is useful in image processing? [3] c) Explain about alpha-trimmed mean filter? [4] d) What is meant by pixel depth? Explain. [3] What is image compression? Why it is needed? Explain. [4] f) Explain the effect of noise on edge detection. [4] $\underline{PART-B} (3x16 = 48 Marks)$ a) What are the various fundamental steps in digital image processing? Explain. [8] 2. b) Find the Haar transformation matrix for N = 8. [8] a) Explain image sharpening using laplacian operator. [8] 3. b) With necessary equations, explain about Homomorphic filtering. [8] a) Explain how periodic noise can be reduced using frequency domain filtering. 4. [8] b) What are the different ways to estimate the degradation function? Explain. [8] 5. a) Explain the procedure of converting colors from RGB to HSI. [8] b) Explain about color image sharpening. [8] a) Discuss about wavelet transform in two dimensions. [8] b) What is block transform coding? Explain. [8] 7. a) Explain the following morphological algorithms [8] i) Thinning ii) Thickening b) Explain edge linking using Hough transform. [8]

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IV B.Tech I Semester Regular Examinations, November - 2016

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Time: 3 hours Max. Marks: 70 Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B **** PART-A (22 Marks) a) Explain about image acquisition using a circular sensor strip. [4] b) What are the advantages and disadvantages of local histogram processing when [4] compared to global histogram processing. What is meant by image restoration? [3] d) What is the purpose of color model? Explain. [3] Write the difference between wavelet transform and Fourier transform. [4] Prove that Erosion and dilation are duals of each other. [4] PART-B (3x16 = 48 Marks)a) Explain about image sampling and Quantization. [8] 2. b) Prove that both the 2-D continuous and discrete Fourier transforms are linear operations. [8] a) Explain the concept of Unsharp masking and Highboost filtering. [8] b) Explain image sharpening using Butterworth highpass and Gaussian highpass filters. [8] a) What are the different types of mean filters used for noise reduction? Explain. [8] b) Explain about image restoration using minimum mean square error filtering. [8] a) Explain the procedure of converting colors from HSI to RGB. 5. [8] b) Discuss about noise in color images. [8] Compute the Haar transform of the 2 x 2 image [8] With an example, explain Huffman coding. [8] 7. a) With necessary figures, explain the opening and closing operations. [8] b) Discuss about region based segmentation. [8]